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Analysis of Power Optimization of Serial Communication Protocol-Memory–Switch Interface

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Abstract:- Power consumption has rapidly risen to an intolerable scale. This results in both high operating costs and high failure rates so it is now a major cause for concern. It is imposed new challenges to the development of high performance systems. Dynamic power can contribute up to 50% of the total power dissipation.In this paper; we first review the basic power management techniques to reduce the dynamic power consumption techniques like clock gating & frequency scaling. Clock-gating is the most common RTL optimization for reducing dynamic power. We have been also studied I^2C and SPI are the most commonly used serial protocols for both inter-chip and intra-chip low/medium bandwidth data-transfers. Both protocols are well suited for communications between integrated circuits for slow communication with on-board peripherals.

Keywords:- Register Transfer Level (RTL) Inter- Integrated Circuit (I^2C), Serial Peripheral Interface (SPI).

I. INTRODUCTION

Today consumers demands more functionality, speed, energy efficient and power optimized device. A system consists of a set of components that provide a useful behavior or service. Power dissipated on clock-lines in a logic chip is approximately 30-50%. Clock signals have been a great source of power dissipation because of high frequency & load. Clock signals do not perform any computation & mainly used for synchronization. Hence these signals are not carrying any information. Gated-clock is one of the most important techniques to reduce power dissipation. By the gated-clock technique, power dissipated on clock lines including synchronous storage elements such as flip-flops and latches can be saved by shutting off the clock of devices when there is no function required. To increase the speed, we have studied two communication protocols SPI & I^2C. Both SPI and I^2C offer good support for communication with low-speed devices, but SPI is better suited to applications in which devices transfer data streams, whereas I^2C is better at multi-master "register access" applications**.**

II. LITERATURE REVIEW

[1] In this paper we studied that the power consumption of AHB SPI-Master is being reduced by using RTL (Register Transfer Level) clock gating technique. Dynamic power can contribute up to 50% of total power. The RTL clock gating technique is used for reducing dynamic power consumption. SPI (Serial Peripheral Interface) is a serial interface which facilitates the synchronous serial data transfer between 2 devices. Dynamic power consumed by the gated clock design is low as compared to non gated clock design.

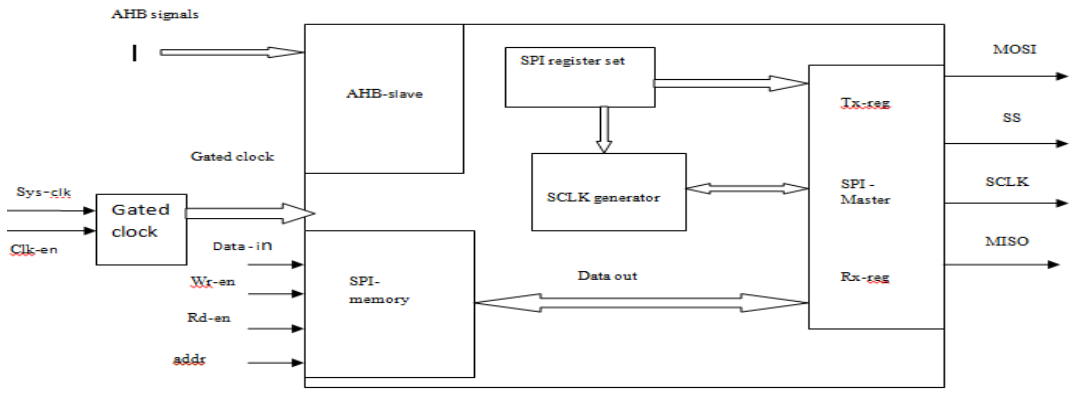

Fig.1.1.AHB-Slave SPI-Master interface diagram with gated clock.

[4] this paper shows that I^2C (Inter Integrated Circuit) and SPI (Serial Peripheral Interface) are the most commonly used serial protocols for both inter-chip and intra-chip low/medium bandwidth data-transfers. This paper contrasts and compares physical implementation aspects of the two protocols through a number of recent Xilinx's FPGA families, showing up which protocol features are responsible of substantial area overhead. The RTL code is technology independent, inducing around 25% area overhead for I^2C over SPI, and almost the same delays for both designs. If data must be transferred at "high speed," SPI is clearly the protocol of choice overI^2C. SPI is full-duplex; I^2C is not. SPI present throughput in the ×100 Mb/s range, but not in Gb/s.[8] this paper describes a design methodology for reducing ASIC power consumption through use of the RTL clock gating feature in Synopsys Power Compiler. This feature causes inactive clocked elements to have clock gating logic automatically inserted which reduces power consumption on those elements to zero when the values stored by those elements are not changing. The methodology was proven in a 200K-gate ASIC, which implemented full scan testing and used RTL clock gating to reduce its power consumption by two-thirds. [9] this paper describes communication protocols the inter-integrated circuit (I^2C) and the serial peripheral interface (SPI) protocols. Both protocols are well suited for communications between integrated circuits for slow communication with on-board peripherals.SPI is a single-master communication protocol. SPI has four signals

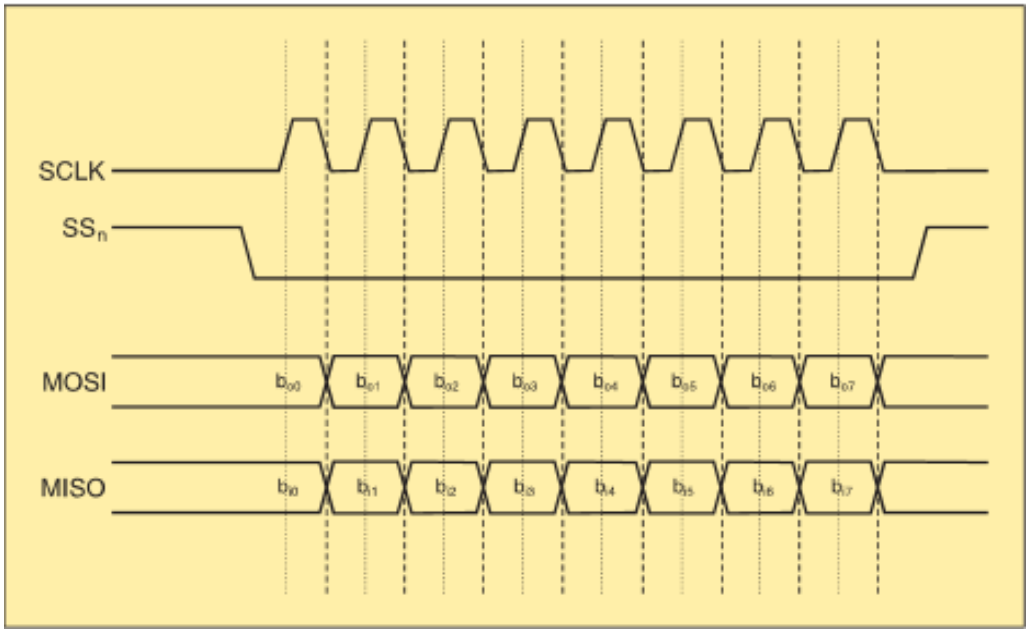

Fig1.2. A simple SPI communication

- A slave select signal (SSn) for each slave, used to select the slave the master communicates with
- A data line from the master to the slaves, named Master Out-Slave In (MOSI)
- A data line from the slaves to the master, named Master In-Slave Out (MISO).
- A clock signal (SCLK) sent from the bus master ‥ to all slaves; all the SPI signals are synchronous to this clock signal

I^2C is a multi-master protocol that uses two signal lines. The two I^2C signals are called serial data (SDA) and serial clock (SCL). There is no need of chip select (slave select). [17] this paper describes Clock gating is one of the power-saving techniques used to save power, clock gating refers to activating the clocks in a logic block only when there is work to be done. Every unit on the chip has a power reduction plan, and almost every Functional Unit Block (FUB) contains clock gating logic. This paper investigates the various clock gating techniques that can be used to optimise power in VLSI circuits at RTL level. [5] This paper describes clock gating is an effective technique for minimizing dynamic power in sequential circuits. Applying clock-gating at gate-level not only saves time compared to implementing clock-gating in the RTL code but also saves power and can easily be automated in the synthesis process. This paper presents simulation results on various types of clock-gating at different hierarchical levels on a serial peripheral interface (SPI) design. In general power savings of about 30% and 36% reduction on toggle rate can be seen with different complex clock- gating methods with respect to no clock-gating in the design.

III. ANALYSIS USING DIFFERENT TECHNIIQUES AND METHODS

[1] This paper describes the comparison between gated clock design and non- gated clock designs. The following table shows comparison of Dynamic power, LUTs and registers used by both the designs.

Table1.1. Comparison for 50 MHz clock

Sr. No.	Features	Non-Gated Clock	Gated clock
1.	Dynamic Power (mW)	12.4	4.9
2.	Number of LUTS	148	145
3.	Number of Registers	35	35

This paper has proven that overall dynamic power is reduced from 12.4 mW to 4.9 mW by the RTL clock gating.

[4] From this paper we have concluded the practical comparative study of I^2C and SPI protocols on different FPGA kits. The paper has shown up the results of an up-to-date FPGA implementation of the slave side of the two standard protocols I^2C /SPI, which are:

- an utilization ratio of 3% and 2% respectively for I^2C Slave and SPI-Slave on the smallest Viertex-5 FPGA device;
- a maximum transfer rate of 75 MBPS for SPI-Slave;
- and an area overhead of 25% for I2C-Slave over SPI Slave
-

Table 1.2 Comparison of occupied slices

		I^2C- Slave		**SPI -Slave**	
Xilinx's FPGA Device	Number of Total Slices	Number of occupied slices	Utilization	Number of occupied slices	Utilization
xc2s50-6tq144	768*	510	66%	363	47%
xc2s50-5tq144	768*	503	65%	354	46%
xc2v80-6cs144	512*	504	98%	366	71%
xc4vlx15-12sf363	6114*	512	8%	360	5%
xc5vlx30-3ff324	4800*	187	3%	141	2%

Table 1.3 Comparison of delays

	I^2C- Slave		**SPI -Slave**	
Xilinx'sFPGA Device	Clock –To- Setup paths	All Paths	Clock –To- Setup paths	All Paths
xc2s50-6tq144	12.079ns	19.616ns	12.234 ns	17.042 ns
xc2s50-5tq144	7.636 ns	14.996 ns	7.835 ns	12.089 ns
xc2v80-6cs144	6.483 ns	12.806ns	6.604 ns	10.234 ns
xc4vlx15-12sf363	4.863 ns	9.572 ns	5.006 ns	8.880 ns
xc5vlx30-3ff324	3.606 ns	7.998 ns	3.303 ns	6.971 ns

[8] Compares the current consumption of gated clock design and clock design.

Table 1.4 Current consumption analysis of clock gated design

Component	Current consumption of Non-Gated clock	Reduced consumption using Gated clock
Clock Tree	36mA	0%
RAMs	0mA	100%
Flip-flpos	32mA	81%
Combinational circuitry	10mA	0%
Total	78mA	72%

This paper has proven that by using clock gating dynamic current consumption of a 200K- ASIC reduced from 280mA to 78mA [9] This paper describes the two communication protocol I^2C and SPI. According to bus topology/routing I^2C is a winner over SPI. If data must be transferred at "high speed", SPI is

choice over I^2C because SPI is full -duplex .This paper prove that when there is a need to implement a communication between an integrated circuit such as microcontroller and a set of relatively slows peripherals, there is I^2C and SPI perfectly fit the bill.
[17] This paper proves that by using RTL clock gating and SPI design power savings of about 30% and 36% with different clock gating techniques in VLSI circuits at RTL level.

IV. CONCLUSION

This paper reviewed techniques and two communication protocols for data transmission for power-efficient system design. Clock gating is the most effective technique to reduce the dynamic power. Both SPI and I^2C offer good support for communication with low-speed devices, but SPI is better suited to applications in which devices transfer data streams, whereas I^2C is better at multi-master "register access" applications.

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