Solar Panel Using Active Stacked Npc Multi Level Converter

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Abstract:- In this project, the operation and the features of a new three-level converter are presented with PV source and boost converter. The proposed topology was named three-level active-stacked neutral point clamped. It is a derivative of the 3L-SNPC structure, having two additional active switches connected anti parallel with the clamp diodes. The main advantage of 3L-ASNPC converter is the reduction of the average switching frequency for all power devices. In the same time, the apparent switching frequency of the output voltage is doubled.

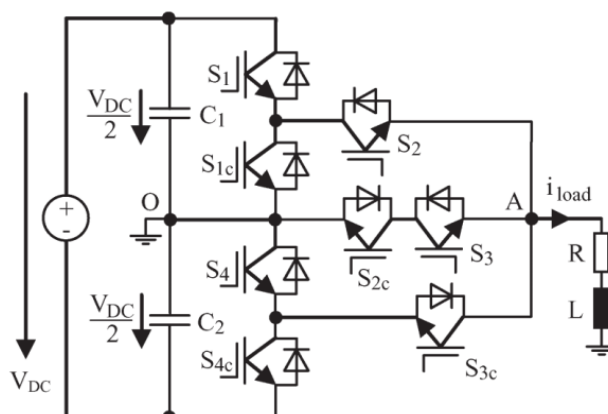**Keywords:-** Multilevel converter solar panel rectifier matlab/Simulink

Fig.1.1

I.   INTRODUCTION

Multilevel structures have been studied for over 25 years, and they represent an intelligent solution to connect serial switches [1]–[9]. The first developed topology consisted of a serial connection of single-phase inverters with dc separate sources [10]–[14]. This structure was followed by a stacked commutation cell concept in order to obtain a multilevel conversion [stacked cells (sc)] [15]–[17].following the sc structure, a new multilevel neutral-point-clamped (npc) topology was developed [18]. The three-level npc (3l-npc) converter is a very popular multilevel structure, being a particular way of implementing the 3l-sc topology. the role of the middle switches in the sc structure is taken by the inner switches and by the two clamp diodes [19].later, another invention introduced the concept of multilevel converter with flying capacitors (fcs) [20]–[24]. The additional expense of fcs, particularly at low and moderate switching frequencies (200 hz–1 khz), is the main disadvantage of the fc topology.

II.   PROPOSED 3 L-ASNPC CONVERTER

Static converter design has to ensure that, in all specific operation conditions, the junction temperature of power devices does not exceed the admitted limits. The junction temperature of each power device is a direct consequence of conduction and switching losses. A better temperature distribution enable substantial increase of the converter's output power at nom- operation or alternatively an increase of the switching frequency [25], [26].The unequal loss distribution among the semiconductors represents one major disadvantage for the 3L-SC and 3L-NPC converters. A better balancing of total losses in power devices has been obtained by developing 3L-active NPC (3L-ANPC) and 3L-stacked NPC (3L-SNPC) topologies [27]–[29].In [28], a feedback-controlled loss balancing system has been proposed for the 3L-ANPC structure. Based on an online estimation of junction temperatures, appropriate commutations are selected in real time such that the hottest devices are not stressed with significant switching losses. This special modulation leads to the balance of junction temperatures of power devices and modifies the output voltage spectrum. However, the control requires a notable amount of

additional computational power, mainly for junction temperature estimation. Drawbacks are the higher cost and the increased control complexity.
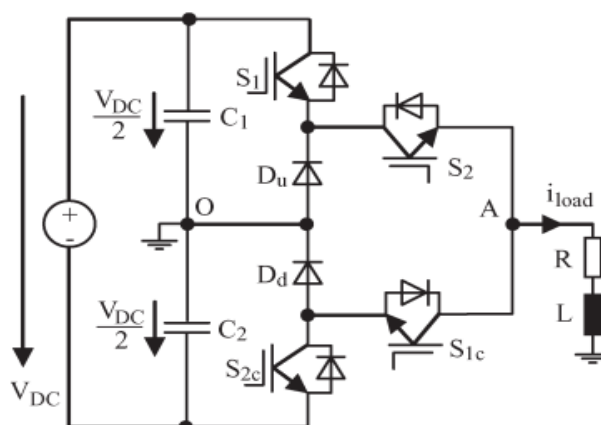

Fig: 1.2

TABLE I

SWITCHING SEQUENCES OF A 3L-NPC CONVERTER

Output Voltage (v_{A0})	Switching State	Switch Sequence			
		S_1	S_{1c}	S_2	S_{2c}
$V_{DC}/2$	P	1	0	1	0
0	O	0	1	1	0
$-V_{DC}/2$	N	0	1	0	1

The 3L-ANPC and 3L-SNPC have more zero switching states that can be used to double the apparent switching frequency [30], [31]. Due to the structural particularities, some power devices switch only on a half cycle, while others switch on the entire cycle. These last ones have the biggest switching losses, being the most stressed power devices that limit the maximum switching frequency or the maximum power output. In this paper, a new three-level converter is presented (Fig. 1).The proposed topology is named 3L-active-stacked NPC (3L-ASNPC). It is a derivative of the 3L-SNPC structure, having two additional active switches connected anti parallel with the clamp diodes.

The main advantage of the 3L-ASNPC converter is the half reduction of the average switching frequency on the entire cycle for all the power devices. In the same time, the apparent switching frequency of the output voltage is twice the switching frequency. Experimental and simulation results are shown in order to validate the proposed topology and the analysis of the switching states.

Existing system limitation:
- The 3L-ANPC and 3L-SNPC have more zero switching states that can be used to double the apparent switching frequency.
- Due to the structural particularities, some power devices switch only on a half cycle, while others switch on the entire cycle.
- These last ones have the biggest switching losses, being the most stressed power devices that limit the maximum switching frequency or the maximum power output.

Proposed system merits:
- A new three-level converter is presented.
- The proposed topology is named 3l-active-stacked NPC (3l-asnpc).
- It is a derivative of the 3l-SNPC structure, having two additional active switches connected anti parallel with the clamp diodes.
- Solar panel will be added.

III. CIRCUIT DIAGRAM EXPLANATIONS

The classical 3L-NPC converter (Fig. 2) is a very popular multilevel structure used in high-power medium-voltage applications. In this circuit, the dc supply voltage is split into three levels by two series-connected capacitors.

By using a sinusoidal pulse width modulation (PWM) strategy, it is observed that the 3L-NPC topology has only three commutation states: P, O, and N (Table I). Switches S1, S 1c,S2, and S 2 care complementary controlled on the entire cycle.

A cycle represents a period of the reference voltage. The states P and N correspond to a direct connection of the load at the dc supply voltage. The state P(Vdc/2) is obtained by turning on switches S 1 and S 2, while the state N (−V dc /2) is obtained by turning on S1c and S 2c . The inner switches S 1c and S 2 are turned on in order to obtain the state O. In this case, the inductive load current passes through two different paths, depending on its direction. The positive load current passes through Du and S 2 , while the negative load current passes through Dd and S 1c .
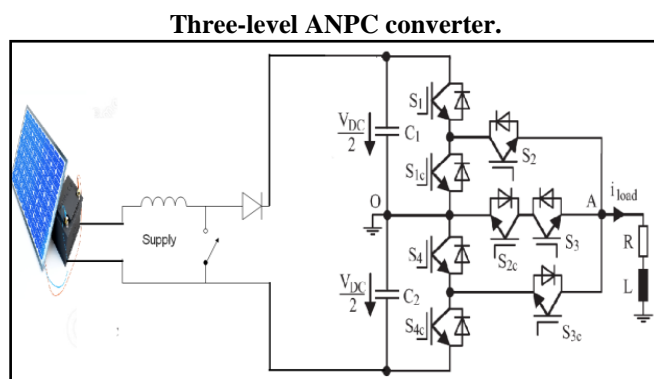
Three-level ANPC converter.

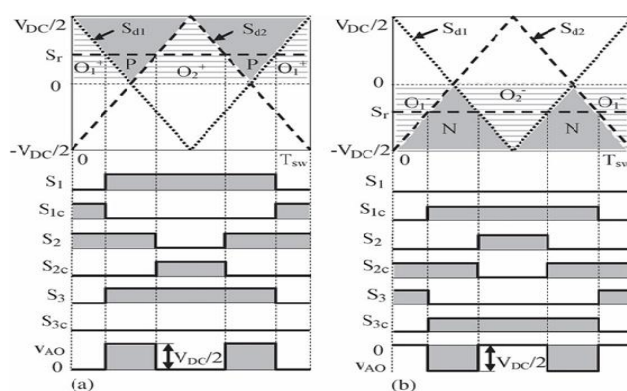**Fig: 3.1.1Circuit Diagram**

Fig: 3.1.2

The control of power devices depends on the sign of the reference voltage. When the sinusoidal reference voltage is positive, the control of power devices S1 and S 1c is made at switching frequency (f sw), while S 2 is turned on, and S 2c is turned off. When the sinusoidal reference voltage is negative, the control of power devices S2 and S 2c is made at f sw , while S1 is turned off, and S 1c is turned on. As a result, the average switching frequency on a cycle (fav) is equal to half of fsw(fav = fsw/2) , while the apparent switching frequency of theoutput voltage (fap) is equal to fsw(fap = fsw).The 3L-ANPC converter is a derivative of the 3L-NPC topology, having two active switches connected antiparallel with the clamp diodes (Fig. 3). This structure can be controlled using different PWM strategies [30].

The PWM strategy analysed in this paper leads to the doubling of the apparent switching frequency (fap=2f sw). The sinusoidal reference voltage Sr is compared with two carrier waves (S d1 and S d2), phase shifted with half of the switching period (T sw /2) . Following the comparison process,six switching states are obtained: P, O + 1 , O + 2 ,N, O − 1 , and O − 2 (Fig. 4). Switches S 2 and S 2c are complementary controlled on the entire cycle. The control of the other power devices depends on the sign of the reference voltage. When the reference voltage is positive, S 1 and S 1c are complementary controlled [Fig. 4(a)]. S 3 receives the same control as S 1 , while S 3c is turned off. In this case (Sr> 0) , three switching states P, O + 1 , and O + 2 are obtained. Switches S 1 and S 2 are turned on in order to obtain the switching state P. S3 is also turned on, but it

does not influence the paths of the load current [Fig. 5(a)]. The state O + 1 is obtained when S 1c and S 2 are turned on [Fig. 5(b)].
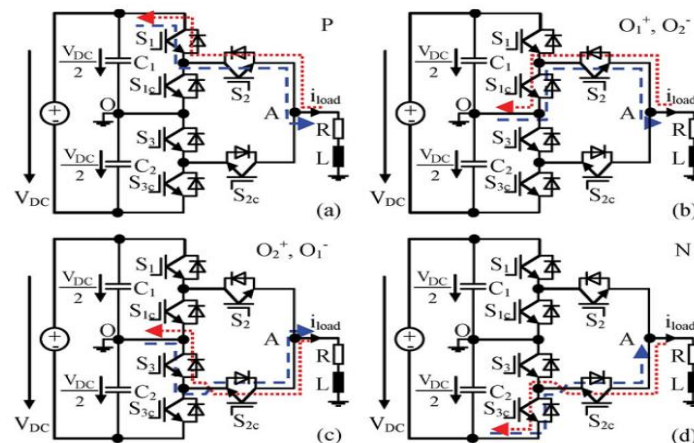

Fig.3.1.3. Current paths for 3L-ANPC converter.(a) State P. (b) States O+1andO□2. (c) States O+2and O□1. (d) State N.

The state O +2 is obtained when S 2c and S 3 are turned on. S1 is also turned on, but it does not influence the paths of the load current [Fig. 5(c)]. When the reference voltage is negative, the other three switching states (N, O − 1 , and O − 2) are obtained [ig. 4(b)]. Switches S3 and S 3c are complementary controlled.

S 1c receives the same control like S3c , while S 1 is turned off. State N is obtained by turning on switchesS2c and S 3c . S 1c is also turned on, but it does not influence the paths of the load current [Fig. 5(d)]. The state O − 1 is obtained when S 2c and S 3 are turned on [Fig. 5(c)], while the state O 2 is obtained when S 1c and S 2 are turned on. S 3c is also turned on, but it does not influence the paths of the load current for O − 2 [Fig. 5(b)].

During the states P and N, two active switches or two diodes are in conduction. In the case of states O + 1 , O + 2 , O − 1 , and O − 2 , one active switch and one diode are in conduction. For the states O + 1 , O − 2 , O + 2 , and O − 1 , the paths of the load current are the same. The switches can be grouped in three pairs: S 1 −S 1c , S 2 −S 2c,, and S 3 −S 3c, . These can be complementary controlled and turned off simultaneously (including the dead times intervals), but they cannot be turned on in the same time.

The controls of the outer switches S 1 and S 3c are realized at switching frequency (f sw) only on a half cycle (Fig. 4). As a result, their average switching frequency on a cycle is equal to half of the switching frequency (f av = f sw/2).
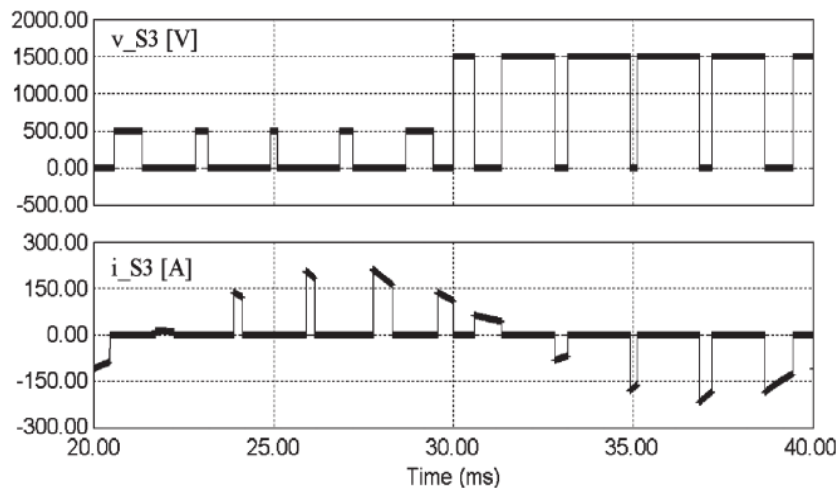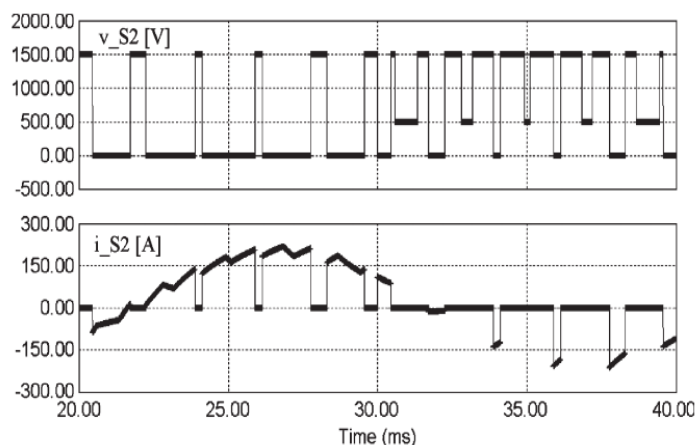

Fig. 3.1.4 shows the simulated waveforms for switch S3 .The frequency of the sinusoidal reference voltage (fR) was set to 50 Hz, and the modulation index (M) was 0.9.
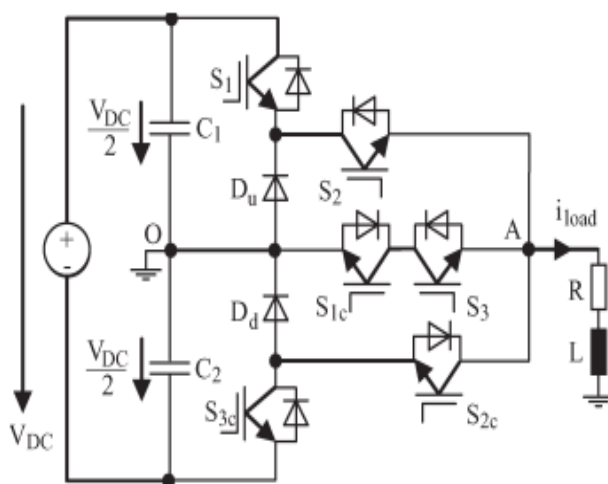
In Fig. 3.1.5. It is observed that S2 operates at f sw on the entire cycle (fav = f sw). S 2c is complementary controlled with S 2 , and it also operates at f sw on the entire cycle (f av = f sw).

It is observed that S 3 commutes at f sw only on a half cycle, whenSr< 0. On the other half cycle,S3 commutes at zero voltage. Thus, the average switching frequency for S3 is considered half of f sw . Due to the symmetry, the average switching frequency for S1c is also considered half of f sw (f av = f sw /2) . Voltage and current simulated waveforms for switch S2 are shown

The 3L-SNPC converter (Fig. 8) is a derivative of the 3L-SC and 3L-NPC topologies [29] and can be controlled using the same PWM strategy shown in Fig. 4. It presents the same advantage of doubling the apparent switching frequency (f ap =2f sw) like the 3L-ANPC topology.

Switches S 2 and S 2c are controlled on the entire cycle with f_{sw} (f_{av} = fsw), while the other ones (including the clamp diodes Du and Dd) commute at f_{sw} only on a half cycle (f_{av} = f Sw /2) . The existence of a single zero switching state represents a limitation of the 3L-NPC structure that has direct consequences on the total loss distribution among the switches [27], [30]. The operation of S2 and S2c at f sw on the entire cycle is also a structural limitation of the 3L-ANPC and 3L-SNPC converters. In order to balance the average switching frequency for all the power devices, a new multilevel converter is proposed.

3. NEW 3L-ASNPC CONVERTER

The 3L-ASNPC converter (Fig. 1) is a derivative from the 3L-SNPC structure, having two additional active switches connected ant parallel with the clamp diodes. All the switches support a voltage equal to V Dc /2. The proposed topology has more degrees of freedom in comparison with the 3L-ANPC and 3L-SNPC converters. The proposed PWM strategy (Fig. 9) allows an average switching frequency that is equal to half of the switching frequency (f av = f Sw /2) for all the power devices. In the same time, the apparent switching frequency of the output voltage is twice the switching frequency(fap=2fsw). In order to emphasize the advantages, the switching states and sequences are analyzed at one switching period T sw for each polarity of the reference voltage.
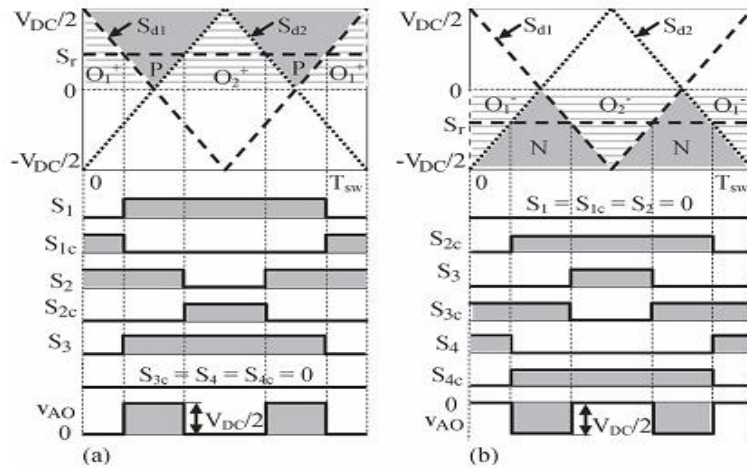
Fig.3.2.2. Proposed PWM strategy for 3L-ASNPC converter. (a) Sr> 0.(b) Sr< 0.

TABLE II
SWITCHING SEQUENCES OF A 3L-ASNPC CONVERTER

Output Voltage (v_{AO})	Switching State	Switch Sequence							
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}	S_4	S_{4c}
$V_{DC}/2$	P	1	0	1	0	1	0	0	0
0	O_1^+	0	1	1	0	0	0	0	0
	O_2^+	1	0	0	1	1	0	0	0
	O_1^-	0	0	0	0	0	1	1	0
	O_2^-	0	0	0	1	1	0	0	1
$-V_{DC}/2$	N	0	0	0	1	0	1	0	1

The reference voltage S r is compared with two carrier waves (S d1 and S d2) that are phase shifted with T sw /2. Following the comparison process, six switching states are also obtained: P,O+1, O+2,N, O−1 , and O−2(Table II) When the reference voltage is positive, S1 , S 1c , S 2 , and S 2c are complementary controlled [Fig. 9(a)]. The other power devices (S 3 , S 3c , S 4 , and S 4c) have a particular control. S 3 receives the same control like S 1 , while S 3c , S 4 , and S 4c are turned off. The control of S3 does not influence the paths of the load current in the state P, but it contributes in obtaining the state O + 2 . When the reference voltage is negative, S3 , S 3c , S 4 , and S4c , are complementary controlled [Fig. 9(b)]. The other power devices (S 1 , S 1c , S 2 , and S 2c) have also a particular control.S2c receives the same control likeS 4c , while S 1, S 1c,and S2are turned off. The control of S 2c does not influence the paths of the load current in the state N, but it contributes in obtaining the state O – 2.
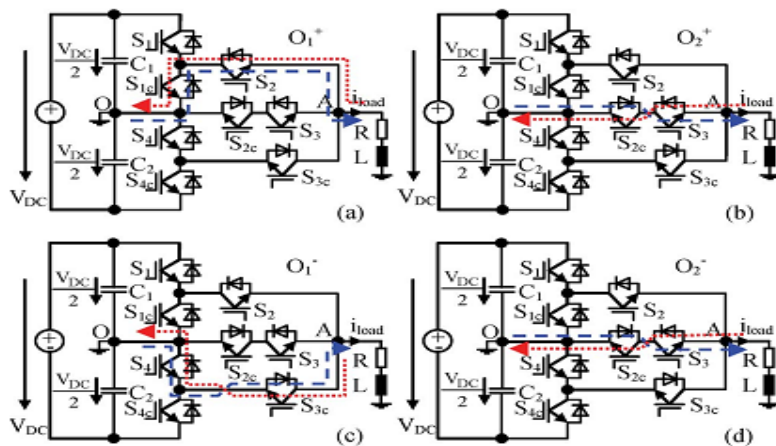

Fig:3.2.3.Current paths corresponding to the states O+1, O+2, O □1, and O □2.
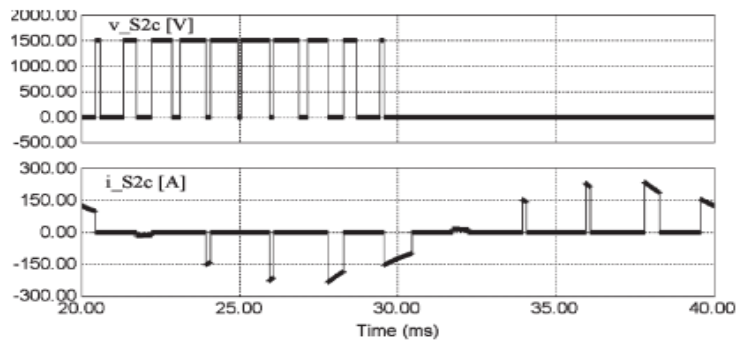
Fig: 3.2.4

A. Switching States State P is obtained by turning on switches 1 and S 2 . S 3 is also turned on, but it does not influence the paths of the load current. In order to obtain the switching state N, switches S3c and S 4c are turned on. S 2c is also turned on, but it does not influence the paths of the load current. The distribution of the conduction losses during states P and N cannot be influenced. For the zero-voltage level, four different control sequences are used. The distribution of the conduction losses during the zero states can be controlled by selecting the upper (S1c −S 2), lower (S4 −S 3c), or middle (S2c −S 3) current paths. During the zero states, one active switch and one diode are in conduction. Even if more than two devices turn on, only one active switch and one diode will be in conduction, depending on the load current direction.

The zero states O + 1 and O + 2 are obtained when the reference voltage is positive, while the states O 1 and O − 2 are obtained when the reference voltage is negative. The zero stateO + 1 is obtained when switches S 1c and S 2 are turned on, while the others are turned off [Fig. 10(a)]. The state O + 2 isobtained when S 2c and S 3 are turned on. S 1 is also turned on, but it does not influence the paths of the load current [Fig. 10(b)]. The other switches (S1c , S 2 , S 3c S 4 , and S 4c) are turned off.

The state O −1is obtained when switches S3cand S 4 are turned on, while the other ones are turned off [Fig. 10(c)]. zero switching state O − 2 is obtained when S 2c and S 3 are turned on. S 4c is also turned on, but it does not influence the paths of the load current [Fig. 10(d)]. The other switches (S1 , S 1c , S 2 , S3c , and S 4) are turned off, and the paths of the load current are similar to the state O + 2 . The switches from the middle side (S2 cand S 3)havea particular control in reducing their average switching frequency on the entire cycle (f av = f sw /2) . When the reference voltage is negative, S2c receives the same control like S 4c , and it commutes at zero voltage (Fig. 11). When the reference voltage is positive, S3 receives the same control like S1 , and it also commutes at zero voltage.

B. Commutations

The commutation to or from the zero states O−1, O− 2, O+1, and O+ 2determine the distribution of the switching losses. Having the same operation conditions and the same features of power devices, the proposed PWM strategy has the same efficiency as the other analysed 3L structures. The four zero switching states are investigated sub sequent.

 For the commutation P →O+1, the phase current is com-mutated to the upper current path (S1c −S 2). First, S1has to be turned off, and then, (after a dead time) S1cis turned on. For the commutation O+1→P, switch S1cis turned off first, and then,(after a dead time) S1is turned on.
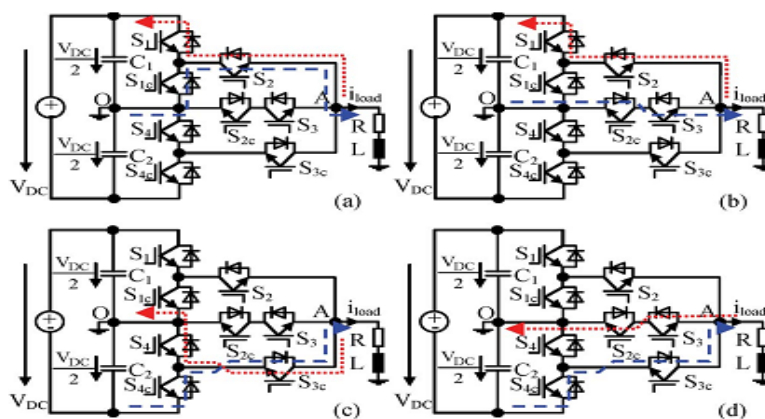

Fig: 3.2.5

The paths of the load current during the dead time (S1and S 1care turned off) are shown in Fig. 12(a).The commutation P →O+2differs from the commutation P →O+1. In this case, the phase current is commutated to the middle current path (S2c −S 3). S2has to be turned off, and then,(after a dead time) S2cis turned on. For the commutation O+2→P, S2chas to be turned off, and then, S2isturned on.
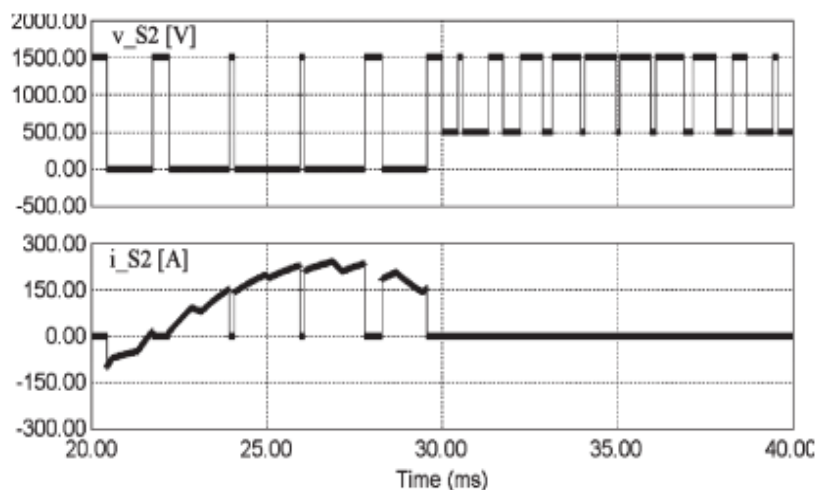

Fig: 3.2.6

The load current paths during the dead time (S2 and S2 care turned off) .The voltage and current waveforms of S2on a cycle are shown in Fig. 13. It is observed that S2commutes at fs won a half cycle when Sr> 0. On the second half cycle (Sr< 0), the load current does not pass through S2. Due to the symmetry of this topology, switch S2c has a similar operation. Through the commutation N →O − 1 , the load current is commutated to the lower current path (S4 −S 3c).First, S4c is turned off, and S 4is turned on after a dead time. For the commutation O 1 →N, switch S 4 is turned off first, and then, (after a dead time) S 4c is turned on. The paths of the load current during the dead time (S4 and S 4c are turned off) . During the commutation N →O −2, the load current is commutated to the middle current path(S2c −S 3). S 3c has to be turned off, and then, (after a dead time) S3 is turned on. In the case of commutation O − 2 →N, S 3 is turned off, and S 3c is turned on after a dead time. Fig. 12(d) shows the load current paths during the dead time (S 3 and S 3c are turned off). In conclusion, each power device of the proposed structure operates at f sw only on a half cycle, and the average switching frequency on the entire cycle is equal to half of the switching frequency (f av = f sw /2) . In the same time, the apparent switching frequency of the output voltage is twice the switching frequency (fap =2f Sw). This advantage leads to a better balancing of the total losses in power devices.

3.3 Solar energy

Solar Energy is about the future as well as the present. With unlimited potential, Solar Energy is a clean, efficient, and sustainable form of renewable energy. Solar Energy in the near future is also a sound financial decision. With Solar panels powering your home, you'll see this every month when your electricity bill arrives. Finally, Solar Energy is a green decision - you'll feel good knowing that you will leave the world a greener, better place for your children.

Today, the worldwide demand for solar photovoltaic (PV) energy is greater than supply. It is one of the fastest growing forms of renewable energy. As manufacturing becomes more efficient, the cost of PV systems continues to drop. Prices have reduced 25 fold over the last 20 years.

Commercially, even electrical utilities are looking to Solar for a more stable cost structure. Research has shown that solar can even be effective in Northern climates. In California, electricity rates are increasing at a rate of 6.7% per year. Solar provides a hedge against future rate hikes. And in many countries, you can sell your surplus electricity back to the utility, generating a credit on your bill.

Not only is solar affordable, it is even more economical when you consider the alternative: the high costs of fossil fuel pollution and global warming. In solar energy scored higher than all other forms of energy when participants were asked what type of energy is best for future generations. Photovoltaic systems produce electric power with no carbon dioxide (CO_2) emissions. The Carbon emission offset is calculated at approximately 7.5 tons of CO_2 over the twenty-five year guaranteed life of one PV module
All in all, solar photovoltaic energy generation has a very bright future indeed.

Photovoltaic Anyone who has used a modern mathematical calculator can grasp the concept of photovoltaic (PV). It is simply the process of converting energy from the Sun into electricity that can power everything from household appliances and lights to commercial buildings and power plants.

In precisely the same way as the small solar cells on hand-held calculators eliminate the need for batteries, PV can provide the world with a clean, reliable source of electricity and reduce our reliance on ever-depleting fossil fuels.

The PV technology of the 21st century makes it possible. It employs layers of micro-fine crystalline silicon to convert ordinary sunlight into small electrical charges. This process is then multiplied thousands of times over to create, smaller than ever before, modules and systems that can generate enough electricity to power entire towns.

It's important to note that PV is different from the solar thermal energy used for heating or in hot water production. A single PV cell consists of two or more thin layers of semi-conducting material, most commonly crystalline silicon. When the silicon is exposed to light, small electrical charges are generated and conducted away by metal contacts as direct current (DC).

In order to maximize energy collection and conversion, single cells are connected together and housed in a module. These modules are the building blocks of the PV systems and are, in turn, connected together to generate usable volumes of electricity. In some instances, an inverter is also used to convert high voltage DC into lower voltage AC power.

IV.   NEUTRAL POINT CLAMPED MULTI-LEVEL CONVERTER

Multilevel topologies provide a clever way of connecting switches in series, thus enabling the processing of voltages that are higher than the device rating. The industry need for medium voltage drives has triggered considerable research in this field, in which most applications include drives for pumps, blowers, compressors, conveyors, and the like. In general, multilevel converters are effective means of reducing harmonic distortion and dv/dt of the output voltages, which makes this technology applicable to utility interface and drives.

There are a limited number of topologies that provide multilevel voltages and are suitable for medium voltage applications. The most known topologies are the neutral-point-clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge multilevel converters. Other topologies such as the hybrid converters have been proposed as well, but they are not fully accepted for industrial applications. The NPC multilevel converter shown in Figure 1(a) is a natural extension of the three-level converter presented by Nabae (NPC3L). As can be seen, the multilevel NPC converter requires multiple clamping points to synthesize the different voltage levels across the output. The disadvantage of multiple clamping points is a limitation on the maximum modulation index that is allowed with active power to assure voltage sharing across all the dc link capacitors. Another drawback of the multilevel NPC converter is the need for series connection of the clamping diodes . Figure 1(b) illustrates a five-level floating capacitor converter. By properly using the dc link and floating capacitor voltages, one can synthesize the required voltage levels across the output terminals. An interesting property of the floating capacitor converter is that the redundant switching states can be used to achieve proper voltage control across the floating capacitors. In general, the energy stored in the floating capacitors is a limiting factor to increasing the number of voltage levels, which makes the five-level approach the most practical for industrial applications. An increased number of voltage levels may only be practical from the view point of floating capacitor requirements if the carrier frequency of the converter is increased. However, there are trade-offs that should be observed between carrier frequency and switching losses in the converter. The cascaded H-bridge multilevel converter shown in Figure 1(c) takes advantage of connecting single-phase inverters in series that are fed by independent dc voltage sources. The approach can be extremely modular, and a stair-cased output voltage is produced by adding and/or subtracting the voltages of the single-phase modules. The power flow may be bi-directional if active front-end rectifiers are used in the single-phase modules. Although modular, the cascaded H-bridge multilevel converter requires a complex transformer to provide the various independent dc sources. Based upon the previous description, this paper proposes an active neutral-point-clamped (ANPC) multilevel converter that combines the flexibility of the multilevel floating capacitor converter with the robustness of industrial NPC converters to generate multilevel voltages. The proposed concept is described and supported by simulation results, and experimental validation demonstrates the proposed technology.

3.5 Boost converter

The step-up dc-dc converter is known as boost converter. Its main applications are in regulated dc power supplies and the regenerative braking of dc motors. The average output is always greater than the dc input voltage. The output voltage is controlled by controlling the switch-duty cycle. When the switch is on, the diode is reverse biased, and hence is the output stage. During the switch on mode the inductor gets the energy from the supply and stores it. During \switch o "state, the diode becomes forward biased and the output stage receives the

energy from the inductor as well as the input. Thus the net energy transferred to the output from input is always greater in a given switching cycle.
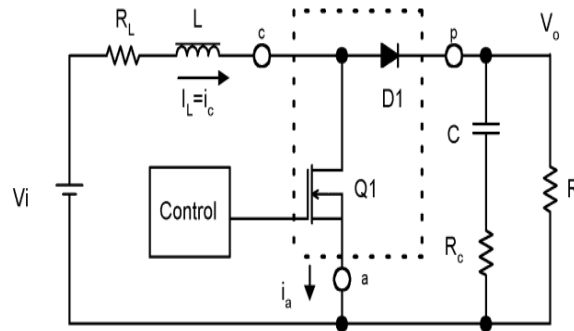

Fig: 3.4.1

A power stage can operate in continuous or discontinuous inductor current mode. In continuous inductor current mode, current flows continuously in the inductor during the entire switching cycle in steady-state operation. In discontinuous inductor current mode, inductor current is zero for a portion of the switching cycle. It starts at zero, reaches peak value, and return to zero during each switching cycle. It is desirable for a power stage to stay in only one mode over its expected operating conditions because the power stage frequency response change s significantly between the two modes of operation.

3.5 Boost Steady-State Continuous Conduction Mode (CCM)

In continuous conduction mode, the boost power stage assumes two states per switching cycle. In the on state, Q1 is on and D1 is off. In the off state, Q1 is off and D1 is on. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuit during each state. Figure 2 shows the linear circuit diagram for each of the two states.
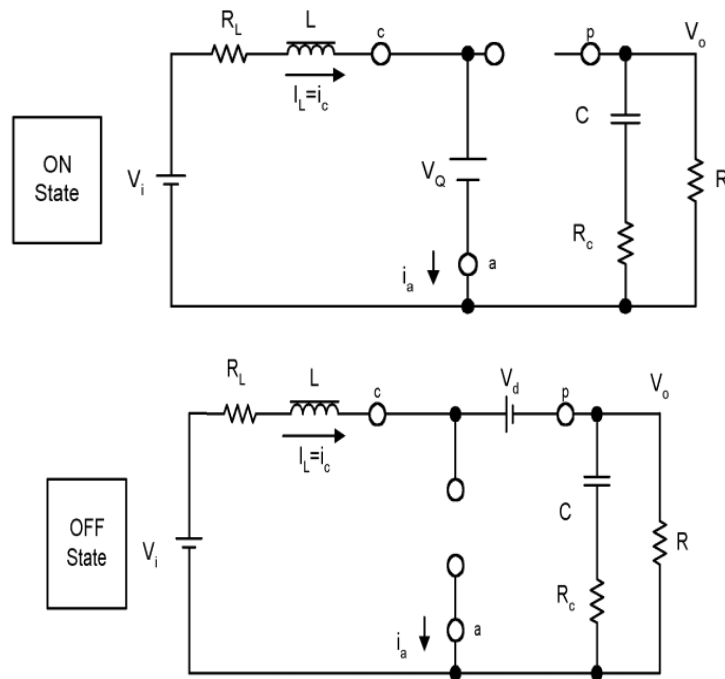

Fig: 3.5.1

3.7 Boost Power Stage States

The duration of the on state is $D \times T_s = T_{ON}$, where D is the duty cycle set by the control circuit, expressed as a ratio of the switch on time to the time of one complete switching cycle, T_s. The duration of the off state is T_{OFF}.
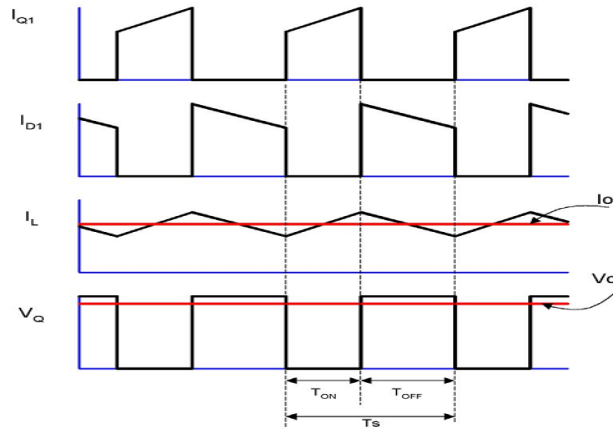
Fig: 3.5.2

3.8 CCM Boost Power Stage Waveforms

Refer to Figures 1 and 2. The inductor-current increase can be calculated by using a version of the familiar relationship:

The inductor current increase during the on state is given by:

The quantity ΔI_L (+) is the inductor ripple current. During this period, all of the output load current is supplied by output capacitor C. The inductor current decrease during the off state is given by: The quantity ΔI_L (-) is also the inductor ripple current.

In steady-state conditions, the current increase, ΔI_L (+), during the on time and the current decrease, ΔI_L (-), during the off time are equa l. Therefore, these two equations can be equated and solved for VO to obtain the continuous conduction mode(CCM) boost voltage conversion relationship

3.9 Boost Steady-State Discontinuous Conduction Mode (DCM)

Figure 4 shows the inductor current condition where the power stage is at the boundary between continuous and discontinuous mode. This is where the inductor current just falls to zero and the next switching cycle begins immediately after the current reaches zero. From the charge and discharge of output capacitor, the output current is given by:
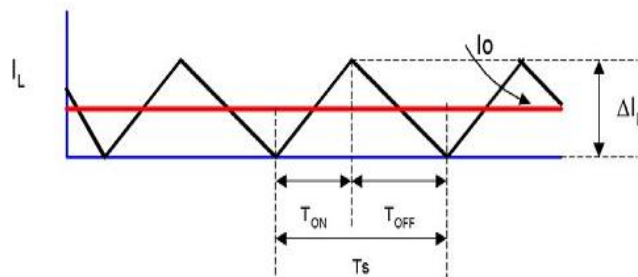

Fig: 3.5.3

Boundary between Continuous and Discontinuous Mode

Further reduction in output load current puts the power stage into discontinuous current conduction mode (DCM). The discontinuous mode power stage input-to-output relationship is quite different from the continuous mode.
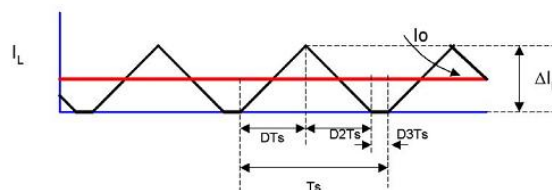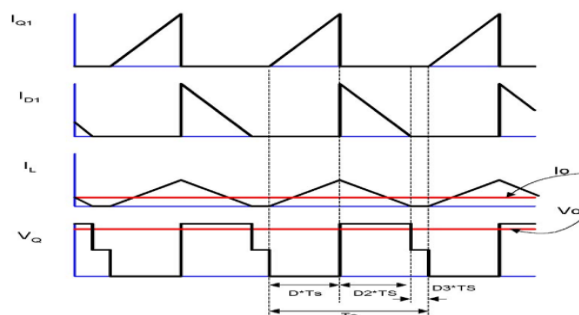

Fig: 3.5.4

Discontinuous Current Mode

The duration of the on state is $T_{ON} = D \times T_S$, where D is the duty cycle set by the control circuit. The duration of the off state is $T_{OFF} = D2 \times T_S$. The idle time is the remainder of the switching cycle and is given as $T_S - T_{ON} - T_{OFF} = D3 \times T_S$. These times are shown with the waveforms in Fig 3.5.5

Discontinuous Mode Boost Power Stage Waveforms

3.6 MOSFET
• The MOSFET device belongs to the unipolar device family, because it uses only the majority carriers in conduction.
• MOSFET stands for metal oxide semiconductor field effect transistor. there are two types of MOSFET depletion type MOSFET enhancement type MOSFET.
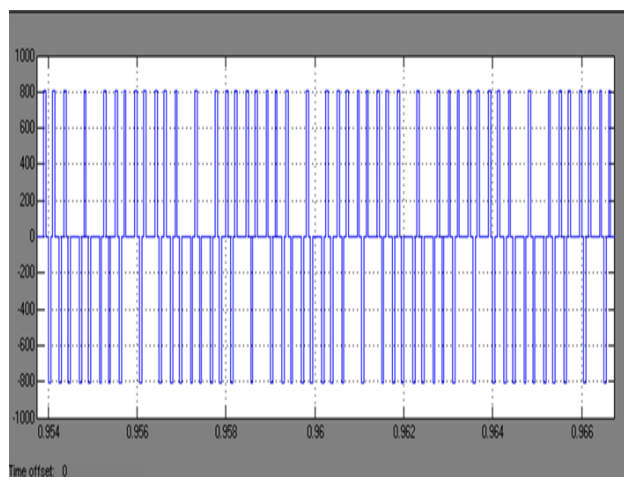
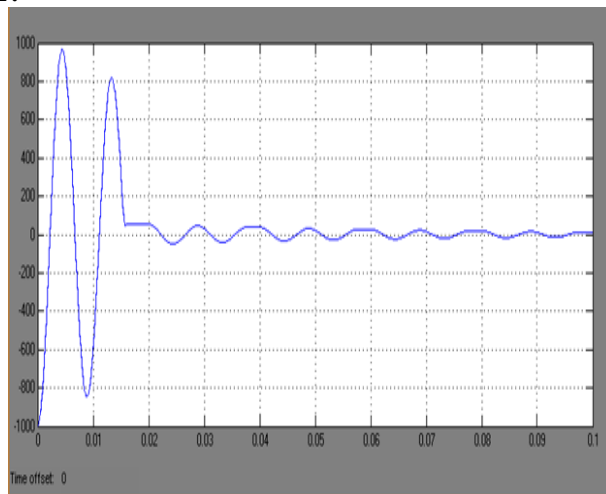**3.7 ADVANTAGES:**
• Half reduction of the average switching frequency on the entire cycle for all the power devices.
3.8 APPLICATION
• High power application
• traction applications
• Industry applications

IV. SIMULATION
WAVE FORMS OUTPUT:

V. CONCLUSIONS

The 3L-ANPC and 3L-SNPC topologies allow the doubling of the apparent switching frequency. In the frame of these structures, there are some power devices that switch only on a half cycle and others that switch on the entire cycle. These last ones severely limit the output power or the maximum switching frequency. In order to overcome this drawback, a new three-level converter has been presented in this project. The proposed topology was named 3L-ASNPC. It is a derivative from the 3L-SNPC, having two additional active switches connected antiparallel with the clamp diodes. The 3L-ASNPC structure has more degrees of freedom and can be controlled using different PWM strategies. The proposed PWM strategy has six switching states and allows the doubling of the apparent switching frequency. Another advantage of the proposed topology is the half reduction of the average switching frequency on the entire cycle for all the power devices and voltage level is boosted using boost converter. This characteristic makes the 3L-ASNPC topology an attractive solution, particularly for medium-voltage and high-power applications.

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