International Refereed Journal of Engineering and Science (IRJES)
ISSN (Online) 2319-183X, (Print) 2319-1821
Volume 3, Issue 5(May 2014), PP.103-109

32-bit ALU with Sleep Mode for Leakage Power Reduction

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Abstract-The work in this project is an attempt to design a 32-bit ALU circuit with sleep mode to reduce leakage power consumption in the circuit. The project uses a local sleep transistors network to achieve sleep mode. During sleep mode, power savings of about 99% in Dynamic power and in Leakage power have been observed. A modified circuit with constant inputs to combinational logic has been experimented and further reduction in leakage and short circuit currents can be observed.
Keywords: Sleep Mode, Leakage power reduction, Sleep transistor design, min leakage constant input vector.

I. INTRODUCTION

The market of portable, battery operated computing devices has grown rapidly in recent years and so the need for Energy efficient design. The mobile computing devices are inactive for a long time and active only for a brief amount of time. So during the inactive state, the devices keep consuming certain power which is dominated by the leakage power consumption of all the components. The designers should provide a mechanism to reduce this leakage power consumption. We are considering the problem of reducing leakage power consumption of ALU by providing a Sleep Mode.

Various methods have been proposed to reduce the leakage power like Reverse Body Bias, Dual-V_{th} domino logic [2], use of Multi Threshold CMOS (MTCMOS)[6], Dynamic Voltage Scaling (DVS), Multi-V_{th} Cell swapping[1] and MTCMOS power gating[5]. One of the most effective solutions is Power gating. This method enables the control logic to turn off selected components in design during the inactive state. The components are invoked again when any activity is detected. Power gating when combined with other techniques such as RBB can achieve more than 100 times less leakage power in sleep mode [5].

Further report is organized as follows. Section 2 summarizes design decisions; section 3 discusses a critical part of power gating i.e. sleep transistor design. Section 4 & 5 discuss experimental setup and section 6 summarizes results. Section 7 concludes the work and talks about future modifications or enhancements.

II. HEADER AND FOOTER DESIGNS AND OTHER DECISIONS

The sleep transistors can be implemented in 2 ways called as Header and Footer types as shown in Figure 1. Though both the types achieve the power gating, they have their pros and cons. We discuss these in this section.

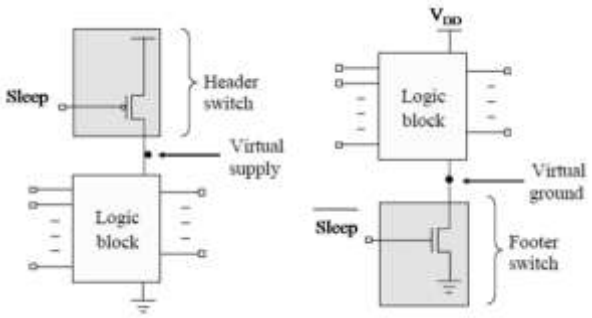

Figure 1: Header and Footer implementations of power gating [5]

The header switch is implemented by PMOS transistors to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of a same size. The NBTI effect increases V_{th} over time and makes PMOS transistor even less leaky. Header switches turn off VDD and keep VSS on. As the result, it allows a simple design of a pull-down transistor to isolate power-off cells and clamp output signals in "0" state. The "0" state isolation is complied with reset state requirement in most designs. The disadvantage of the header switch is that PMOS has lower drive current than NMOS of a same size, though difference is reduced by strained silicon technology. As a result, a header switch implementation usually consumes more area than a footer switch implementation.

The footer switch is implemented by NMOS transistor to control VSS supply. The advantage of footer switch is the high drive and hence smaller area. However, NMOS is leakier than PMOS and application designs become more sensitive to ground noise on the virtual ground (VVSS) coupled through the footer switch. The isolation on "0" state becomes complex due to loss of the virtual ground in sleep mode and necessity of bypassing footer switch to reach permanent VSS. In the following part of the paper, we shall focus on header switch design and implementations.

This work has many transistors to use in the sleep transistor network so considering the area penalty; it is decided to use a footer type of transistor structure.

Also some other design decisions made are discussed here. A Local sleep transistor network is used as opposed to Global or cell level transistors. As the gate count of original circuit is about 1450, a cell based design would require equal number of sleep transistors which is a high area overhead. As this circuit is a pure combinational logic, no data retention technique has been used. The output of a power gated circuit needs to be isolated from the next stage of logic as the crowbar currents may create excessive power consumption in next stage. This is done by using a simple circuits like a isolation cells made by AND or OR. Also, clamped pull-up or pull-down transistors can be used. A level shifter approach is also discussed in [7]. The ALU circuit under experimentation is an isolated block with buffers at SUM output to provide output capacitances so we have not implemented the current isolation circuit.

III. SLEEP TRANSISTOR DESIGN

One of the most critical decisions in power gating is the design of Sleep Transistor. In this work we have considered a worst case scenario of current through the sleep transistor as a design criterion. The Sleep transistor resistance should be large enough in sleep mode to produce a considerable voltage drop, almost equal to VDD, between GND and Virtual GND. Also the on resistance should be as small as possible as it will have the least effect on discharge path delay and hence on the speed of the circuit. But these requirements always contradict each other because a smaller resistance means wider area of transistor which causes more power consumption so there is always a tradeoff between leakage power saving and speed of the circuit.

Considering above worst case current scenario, a Sleep transistor is designed as follows.

Delay of a single gate without sleep mode is given as

$$\tau d = \frac{C_L V_{DD}}{(V_{DD} - V_{tL})^{\alpha}} \quad \text{……. (1)}$$

Where, V_{DD} is the supply voltage, V_{tL} is low level threshold voltages, α is Saturation Velocity Index and C_L is the load capacitance.

If a sleep transistor of High Vt is introduced, we get delay as

$$\tau d^{Sleep} = \frac{C_L V_{DD}}{(V_{DD} - Vx - V_{tL})^{\alpha}} \quad \text{……. (2)}$$

Where, Vx is the drop across sleep transistor while the circuit is in active mode.

Allowing 5% overhead in the delay for this design, we get

$$\frac{\tau d}{\tau d^{Sleep}} = 95\% \quad \text{……. (3)}$$

Solving this equation for α=1.8 gives, the voltage drop across sleep transistor as

$$Vx = 0.0281(V_{DD} - V_{tL}) \quad \text{……. (4)}$$

The current through the sleep transistor is represented approx. by

$$I_{Sleep} \approx \mu_n C_{ox} \left(\frac{W}{L}\right)_{Sleep} (V_{DD} - V_{tL})(V_{DD} - V_{tH}) \text{……. (5)}$$

Where, μ_n is mobility of electrons = 150 $cm^2/V.s$ at 90°C, C_{ox} is oxide capacitance = 19.7 X 10^{-6} F/m for 45nm [4].

So the width over length ratio of a sleep transistor is given by

$$\left(\frac{W}{L}\right)_{Sleep} = \frac{I_{Sleep}}{0.0281 \mu_n C_{ox} (V_{DD} - V_{tL})(V_{DD} - V_{tH})} \text{……. (6)}$$

I_{sleep} is calculated by simulating the ALU circuit without sleep transistor network and finding maximum current that flows through ground. This equation for a 45nm technology related parameters gives a value of

(W/L) = 4774.7 ≈ 4800. This is incorporated in the design as a set of 80 parallel sleep transistors with (W/L) of 60 each as shown in the figure 3.

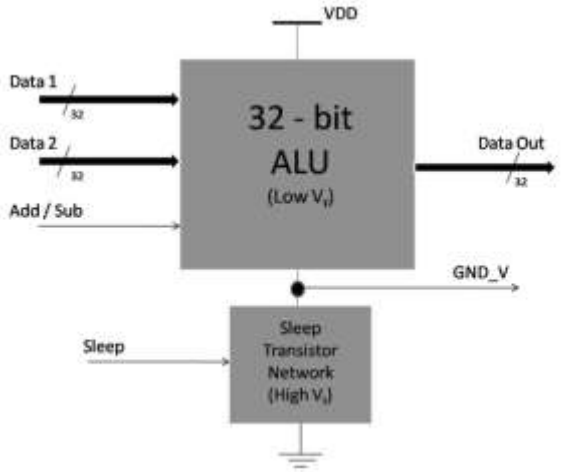

Figure 2: A 32-bit ALU with sleep transistor network as a black box

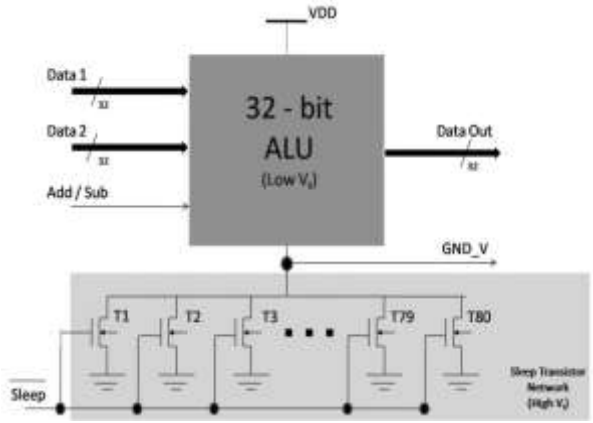

Figure 3: A 32-bit ALU with calculated no. of sleep transistors added to the network

IV. EXPERIMENTAL SETUP

The experimental setup consists of a 32-bit ALU circuit written originally in VHDL and then synthesized to a transistor level net list by using Leonardo Spectrum and Design Architect. The design was synthesized to a 45 nm technology. This design has two 32-bit operand inputs and a Add/Subtract input i.e 65 inputs in total and a 32-bit Sum output port. A set of 200 random vectors were applied to the circuit and it is simulated in HSPICE to get the maximum current through sleep transistor (I_{sleep}) which we have used in Equation (6).

Sleep transistor network is later added to this circuit as shown in figure 3.

A set of experiments were carried out on the circuit to find power savings and response times of the circuit for transitions from sleep to active and active to sleep mode. Following is a list of experiments which were carried out

a. Applied 200 vectors in Active mode i.e. Sleep = '0'
b. Applied 200 vectors in Sleep mode i.e. Sleep = '1'
c. Applied 200 vectors when Sleep signal is changing from 1 to 0 after 100 vectors
d. Applied 200 vectors when Sleep signal is changing from 0 to 1 after 100 vectors

Part a gives an estimation of circuit's Dynamic and Leakage energy in Active mode while part b for the sleep mode. In Part c, circuit changes from Active mode to Sleep mode and we can calculate sleep time while in part d we can calculate wake up time. During the sleep mode, it was observed that a certain vector of 65 inputs has minimum leakage power consumption for a given set. This input vector is recorded for future circuit modification.

V. MODIFIED CIRCUIT (WITH MULTIPLEXERS)

As we will discuss section 6, the simulations in sleep mode show considerable fluctuations in the power consumption of the circuit when the input changes from one vector to other. Leakage currents through the 80 parallel sleep transistor and short circuit currents are some of the possible reasons. A modification in the circuit is discussed which eliminates the change at inputs of ALU and hence reduces leakage and dynamic power even further.

A combinational logic is generally sandwiched between two registers (clocked elements). Also, a sleep mode is accompanied by the clock gating of these registers as their contents do not change during the sleep mode. So during a sleep mode, a combinational circuit practically has a constant input vector at its inputs. This vector determines the leakage power consumed by the circuit. To minimize this leakage power, we can modify the circuit such that it will have a constant and min. leakage power consuming vector at its input.

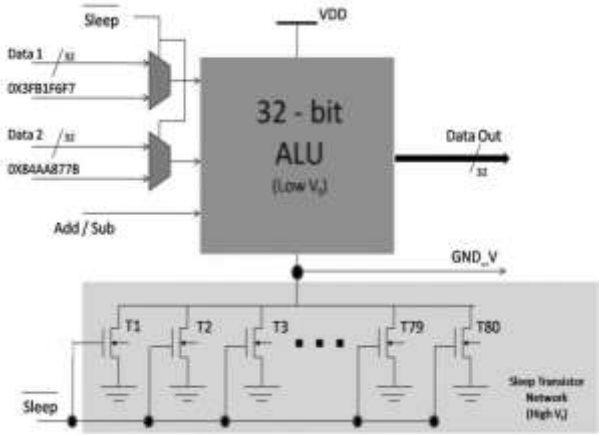

Figure 4: Modified circuit to provide a constant input vector during sleep mode

During the sleep mode, it was observed that certain input pair causes least leakage power in the circuit. As the exhaustive set combinations (2^{65} = 36.9 X 10^{18}) cannot be tested, a minimum leakage vector out of the chosen random vectors is found out. This vector can be used as a constant vector at the input of the circuit and the modification in the circuit to accommodate this feature is as shown in the figure 4.

VI. RESULTS

Results of some of the experiments are shown below.

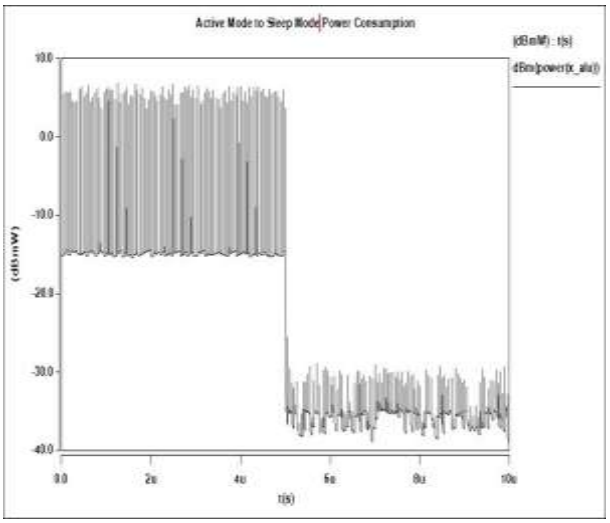

Figure 5: Active to sleep mode transition of ALU. The sleep signal is activated at 5us for this 10us simulation.

As can be seen in figure 5, the dynamic and leakage power consumption in ALU during active mode (0 to 5us) is considerably high as compared to that in sleep mode (5 to 10 us). The sleep mode power consumption though low in average value contains some switching power or short circuit power when the input vectors

change. This also pulls down the virtual ground from 1.1 V to 1.0 volts. Large number of sleep transistors allowing a leakage current and short circuit currents can be some of the dominant reasons of these power peaks.

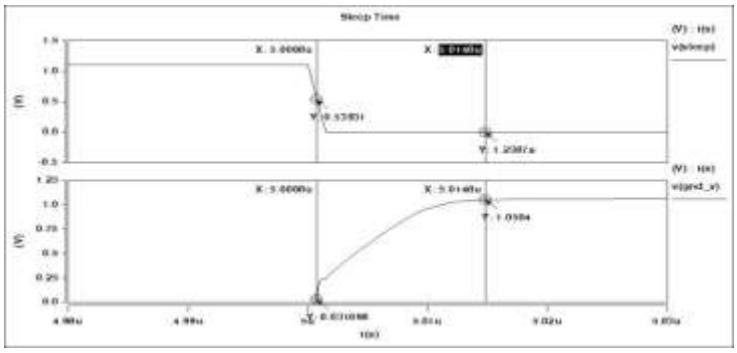

Figure 6: Recording of Sleep time. Sleep signal (top) changes from '1' to '0' and the Virtual ground (bottom) changes from '0' to approximately V_{DD} after sleep time.

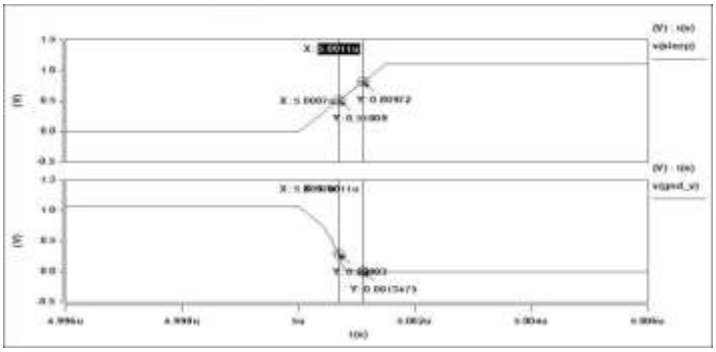

Figure 7: Recording of Wake Up time. Sleep signal (top) changes from '0' to '1' and the Virtual ground (bottom) changes from approximately V_{DD} to '0' after wake up time.

Figure 6 and 7 show results of the experiments which are used to record sleep time and wake-up time given in Table 2. After modifying the circuit with 2 additional multiplexers to hold minimum leakage power vectors at the input of ALU, we ran the same set of 200 vectors from active to sleep mode. The result is as shown in figure 8. Comparing it to the results in figure 5, after 5us the power consumed in ALU is only leakage power and equal to the minimum possible leakage power out of all the 200 vectors.

Another set of experiments of power gating a single logic gate like EXNOR was performed. Effect of sleep transistor sizing and no. of sleep transistors on Dynamic & Leakage power as well as on virtual ground was observed. It was observed that Dynamic and Leakage power increases with increase in sleep transistor size and no of sleep transistors. Also droop in virtual ground during sleep mode and ground bounce during active mode decrease with increase in sleep transistor size and no of sleep transistors.

Table 1 summarizes the dynamic and in Leakage power savings in sleep mode and sleep mode with constant input vector.

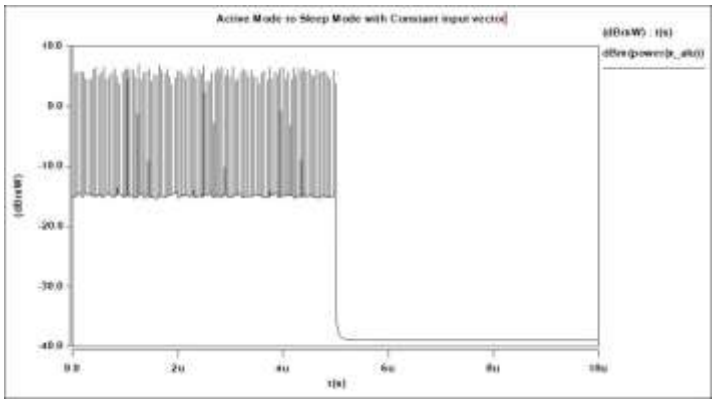

Figure 8: Active to sleep mode transition of ALU with constant input vector during sleep mode. The sleep signal is activated at 5us for this 10us simulation.

Table 1: Summary of power savings in Sleep mode and in Sleep mode with constant input vector as compared to normal mode operation

	Normal (uW)	**Sleep Mode (nW)**	**Power Saving (%)**	**Sleep Mode with Constant Input Vector**	**Power Saving (%)**
Avg. Dynamic Power	660.0	302.204	99.95	0 nW	100
Avg. Leakage Power	34.01	241.32	99.29	127.4 nW	99.61
Peak Power	5040.5	1361.13	99.79	127.4 nW	99.99
Min. Power	29.2549	127.4	99.56	127.4 nW	99.56

Table 2: Summary of overheads caused due to implementation of sleep mode.

Sleep Time	14 nS
Wakeup Time	0.4 nS
Area Overhead	45.5% 1456 → 1456 + 80 (CMOS with W/L = 60)

VII. CONCLUSION & FUTURE WORK

According to the no. of experiments carried out, we can see that Power gating is an effective technique to reduce leakage power consumption of a combinational logic block like ALU during inactive state. Savings can be as much as 99% of the total power consumption with only proper sleep transistor network. The switching currents/ fluctuations can be further reduced by applying a constant low leakage vector at the input of the circuit during sleep mode.

As discussed in the results section, we still observe some dynamic power consumed in the ALU during sleep mode with the change in input due to possible high leakage current or short circuit currents. The investigation of these currents is required and is part of future work. The problem can be solved using constant low leakage vector at the input. Also the area overhead is quite high which can be reduced with selective clustering of transistors in the ALU which is also a part of future work.

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